FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

Structures and methods for Flash memory with low tunnel barrier intergate insulators are provided. The non-volatile memory includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposing the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel barrier intergate insulator. The low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5. The floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator. And, the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.